

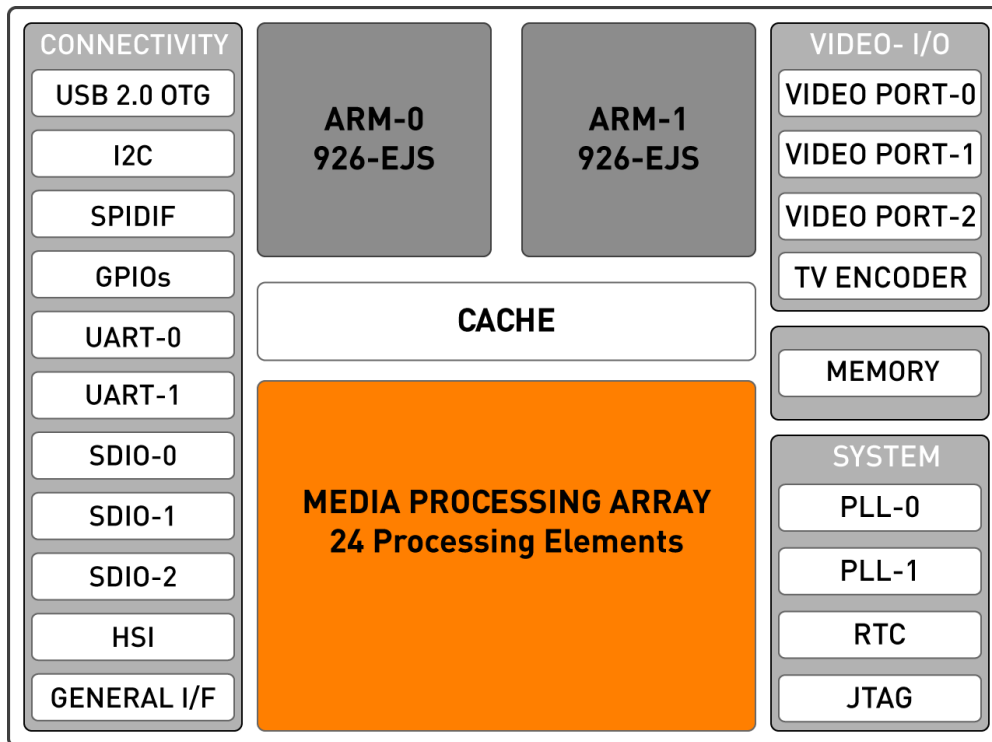


ZMS-05 Media-Rich Applications Processor

ZiiLABS Semiconductor is a pioneering developer of fully programmable, media-rich application processors capable of delivering high-performance application, graphics and multimedia capabilities within a low-power environment

The ZMS-05 multi-core design combines dual ARM® cores with a flexible media processing array to achieve fully balanced acceleration of CPU and media-intensive tasks. A broad range of I/Os and peripheral functions are integrated on-chip to ease system design and reduce BoM costs.

A rich suite of evaluation platforms, SDKs, BSPs and reference designs harness the power and flexibility of ZMS-05's processor and enable OEMs and ODMs to deliver unrivalled media rich products across a broad range of portable and embedded markets.



KEY FEATURES AND ADVANTAGES

• Flexible Media Processing

- High compute density SIMD architecture ideally suited for media processing tasks
- Performance and flexibility to accelerate a wide range of current and emerging standards
- Ideally suited to video, imaging, 2D/3D graphics, audio and signal processing
- Offloads the CPU from intensive media tasks
- Integer and IEEE 32-bit and 16-bit floats

• Dual ARM® processor cores

- Dual ARM926 EJ-S
- Scalable system performance
- Optimal power management

• High-Definition Video

- High resolution 720p decode and encode
- Wide range of video codecs, including;
 - H.264, MPEG 1/2/4, WMV/VC-1 and others
- Integrated HD 1080p analog TV encoder

• High-Fidelity Audio

- High quality audio encode and decode
- Wide range of audio codecs including;
 - MP3, AAC, WMA, AAC, Ogg Vorbis and others
- Special effects

• High Quality Imaging Processing

- Software Defined Imaging Pipeline
- High quality imaging from low cost sensors

• High Quality 2D/3D Graphics

- 2D graphics acceleration
- Powerful floating-point 3D graphics
- Supports OpenGL ES 1.1 and 2.0
- Advanced UI features and experiences

• Ultra-Low Power consumption

• High Level System Integration

Integrated functions and I/O ports help to simply system design and reduce BOM costs, including:

- USB 2.0 OTG, TV encoder, three independent video I/O ports, three SDIO/MMC, I2C, I2S, UARTs, GPIOs, Hi-speed serial, SPDIF and General Interface supporting NAND/NOR flash, IDE, Ethernet, PLLs and RTC.

• Performance

- MPEG-4 AVC/H.264 HD decode
 - Main profile at 30 fps, 8mbps bitstream
- 3D Graphics (OpenGL ES)
 - 42M textured pixels/sec, 21M vertices/sec
- Compute
 - 8GFLOPS, 32GOPS
- Memory bandwidth
 - 2.6 GBytes/sec

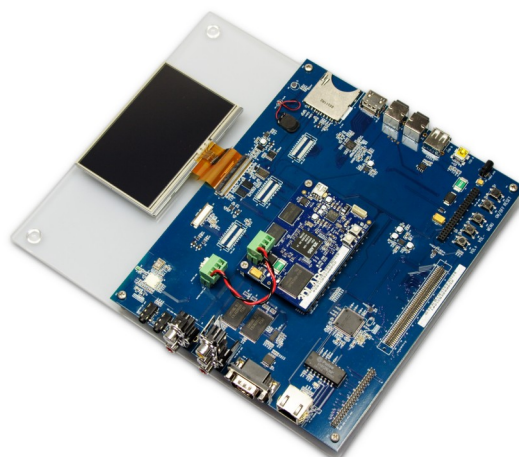
• Applications

The performance, flexibility and low power consumption of the ZMS-05 make it ideally suited to a broad range of portable and embedded applications.

- Portable Media Players
- Mobile Internet Devices
- Portable Navigation Devices
- Video Conferencing
- Video Surveillance
- Automotive Infotainment
- Smartphone and PDA
- IP Media devices
- Digital Signage
- Embedded Systems

- **Dual ARM® 926 EJ processor cores**
 - ARMv5TEJ architecture
 - ARM-0 typically runs OS with ARM-1 acting as an applications co-processor
 - 32-bit ARM instruction set
 - 16-bit Thumb instruction set
 - 32Kbyte instruction cache
 - 16Kbyte data cache.
 - JTAG access to debug registers
 - ARM Jazelle technology
 - Independent interrupt controllers
 - Independent clocks speeds
- **Media Processing Array - Overview**
 - Offloads the CPUs from media-intensive tasks
 - Performance is exposed via optimized high-level APIs, libraries and CODECs
 - Fully programmable with the flexibility to accelerate a wide range of current and emerging media formats, including;
 - Video encode and decode
 - 2D and Vector graphics
 - 3D graphics, programmable floating point vertex and pixel processing
 - Image encode, decode and manipulation
 - Camera processing
 - Audio processing
 - Software GPS
 - Digital Signal Processing
 - Software defined radio
- **Media Processing Array - Architecture**
 - High compute density SIMD architecture
 - 24 Processing Elements (PE) in 3 clusters
 - Each cluster runs the same or independent code
 - Multiple High bandwidth memory paths
 - Advanced hierarchical cache structure
 - Random access to memory per PE
 - Shared access to ARM memory
 - Independent DMA controller per cluster
 - Integer, IEEE 32-bit and 16-bit floating point
 - Pre-emptive task switching
 - Independent frequency scaling
 - Independent voltage domain
- **Memory Interfaces**
 - Mobile SDR, DDR and DDR2
 - x32 and x64 data bus
 - 166/266MHz
 - 1Gbyte address space
 - Automatic power & clock control when idle
 - Self-refresh for hibernate
- **USB 2.0 OTG Controller**
 - Integrated USB 2.0 PHY
 - Full speed and High-speed 480Mbps/sec
 - Device and host
 - 4x bi-directional endpoints
 - Independent DMA controller
- **Advanced power management**
 - H.264 BL 720p video playback in under 300mW
 - 30fps 720p BP, 5mbps, 96KHz AAC
 - Three voltage domains (fabric, array and RTC)
 - Dynamic clock and voltage scaling
 - 16 independent power down regions
 - Multiple clock domains and clock gating
 - Suspend to RAM feature
 - Low power process
- **Three SDIO/MMC Mobile Storage ports**
 - 3x independent mobile storage ports
 - Independent DMA controllers
 - SD/SDIO V2.0, MMC V4.2 and CE-ATA V1.0
 - 1-bit and 4-bit SD card support
 - 1-bit, 4-bit, or 8-bit MMC cards
 - 4-bit or 8-bit CE-ATA devices
 - Control pins, e.g. card detect, write protect
 - 8-bit modes require two SDIO/MMC ports
- **Video Ports**
 - Three independent glue-less, bi-directional ports to external video devices, including; LCD displays, camera sensors and video encoder/decoder devices
 - Independent 12-bit video data-busses with HYSYNC, VSYNC, Valid and Clock per port.
 - 160+MHz pixel clock for high-resolution displays. e.g. 320x240 up to 1080P
 - Formatting and manipulation of video data
 - Color space conversion
 - YUV and RGBA data formatting
 - Independent DMA controller per stream
 - Independent timings per stream
 - Integrated LUT and Gamma control
 - Input and output scaling
 - Compositing and blending of output streams
 - Progressive and Interlaced displays
 - Support for external genlock
 - Unused streams available for GPIO
 - One port shared with on-chip TV encoder
- **Integrated HDTV TV encoder**
 - NTSC, PAL, SECAM
 - High definition: 480p, 576p, 720p, 1080p
 - Standard definition: 480i, 576i
 - RGB and YUV component output
 - 8-bit color components
 - Wide screen signalling and closed captions
 - Macrovision® option
- **General Interface Bus**
 - General purpose, programmable bus for the direct connection to peripheral devices
 - NOR/NAND Flash, IDE and CompactFlash, Ethernet controllers and other peripherals
 - Programmable, multi-protocol bus
 - Programmed IO, Fast PIO and MUX
 - 40-bit address/data bus, plus 17 control pins
 - 8, 16 or 32-bit data
 - Address uses remaining 32, 16 or 8-bits
 - 32-bit multiplexed address/data on same pins
 - 4 concurrent channels from 8 devices
 - Master and slave on all channels
 - Independent DMA controller per channel
 - Boot from device and MLC boot support

- **General Purpose Input/Output**
 - Up to 34 GPIO pins
 - Level and edge sensitive interrupts
- **I²C**
 - Two wire Master/Slave serial interface
 - Standard (100Kb/s) or Fast mode (400Kb/s)
- **High-Speed Serial Port**
 - 200Mhz, 2 or 3 wire serial port
 - 1-bit, 2-bit and continuous bitstream modes
 - Ideal for RF interfaces, e.g. GPS and DVB receivers
- **Two UART Ports**
 - Dedicated DMA channels
 - Hardware flow control of both ports
 - Support SIR/IrDA infrared communication.
 - 3 mbps maximum transfer rate
- **JTAG**
 - Full boundary scan
- **I²S Digital Audio Bus**
 - Independent stereo input and output ports
 - Dedicated DMA
 - 32 KHz -192 KHz
 - 16, 24 or 32 bit word lengths
- **S/PDIF**
 - Sony/Philips Digital Interface for digital I/O
 - Input and output channel with dedicated DMA.
 - 22.05KHz, to 192KHz output
- **PLL Clock Generators**
 - Two low-jitter PLL's up to 666Mhz
 - 17 controllable clocks
 - Independent control and divider
 - Built in crystal or external oscillator
- **Secure Real-Time Clock**
 - Built-in 32.768KHz oscillator
 - 4 general purpose timers
 - Independent voltage domain
 - Tamper detection
 - Wake / Sleep support
- **Security**
 - Unique ID
 - Secure boot from ROM
 - Tamper detect on RTC
- **Physical Characteristics**
 - 464 pin BGA
 - 15x15mm
 - 0.5mm ball pitch
 - 0.8V-1.2V Core
 - 1.8/3.3V IO
 - 1.8V/2.5V Memory
 - 0°C to 85°C
 - RoHS compliant



ZMS-05 EVALUATION MODULE (EVM)

The ZMS-05 EVM provides a complete hardware and software platform for the evaluation and development of a broad range of handheld and embedded products based on the ZMS-05.

See the ZMS-05 EVM Product Brief for additional information.

HARDWARE DESIGN KITS AND BSPs

Registered partners can access Hardware Design Kits and Board Support Packages (BSPs) for the ZMS-05 EVM, including schematics, gerbers and BOMs.

SOFTWARE DEVELOPMENT KIT (SDK)

The ZMS processors are supported by a powerful SDK that enables the rapid development and porting of ARM® based applications that can exploit the highly optimized CODECs, APIs and libraries running on the media processing array.

See the SDK Product Brief for additional information.